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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,370	01/27/2004	Duncan McRae	100303.P1855	1576

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EXAMINER	
NGUYEN, HIEP	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 12/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/765,370	MCRAE ET AL.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 15-30* is/are rejected.

7)☒ Claim(s) *10-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is responsive to the amendment filed on 09-09-05. Applicant's arguments with respect to reference Michail (US Pat. 5,760,649) have been carefully considered but they are not deemed to be persuasive to overcome the reference. Thus, the claims remain rejected under Michail. The rejection changes slightly for clarification.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 20, 21 and 24-27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claim 20, the recitation "said feeding back further comprises **a comparison** of said received output signal to a reference voltage" in indefinite because it is misdescriptive. Figure 4 of the present application shows that the feedback devices (410, 420) are passgates having control terminals connected to the supply voltage and the ground. The passgates are constantly turned on and act as resistances. Therefore, **no "comparison of said received output signal to a reference voltage" is possible.**

Regarding claim 24, the recitation "feeding back to said one or more transistors **a portion** of said output" is indefinite because it is misdescriptive. Figurer 4 or figure 7 of the present application show that the feedback device is resistor (764) that is coupled **directly** from the output of the circuit to the control terminals of the transistors thus, the whole output voltage is fedback not a portion of the output as recited.

Claims 21 and 25-17 are indefinite because of the technical deficiencies of claims 20 and 24.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-7, 9, 15, 17-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Michail et al. (US Pat. 5,760,649).

Regarding claims 1-4, figure 1 of Michail shows a method for dynamically controlling an output driver stage comprising:

sensing a signal from an output (OUTPUT) from said output driver stage (feedback blocks 110, 112); and

controlling said output driver stage based on said sensed signal.

The output driver stage comprises two or more stacked transistors (102, 104 106, 108) configured in a cascode mode. The delay between the sensed signal and the control signal applied to the gates of transistors (106) and (108) is less than two gate delays in time. Note that the feedback blocks comprise resistive elements.

Regarding claims 5-7, figure 1 of Michail shows an apparatus comprising:

means (110, 112) for sensing a signal from an output driver stage; and

means for controlling said output driver stage (106, 108) based on said sensed signal .The means for sensing is selected from the group consisting of a resistive means (110, 112). The output driver stage comprises two or more stacked transistors (102, 104, 106, 108).

Regarding claims 9 and 15, figure 1 of Michail shows a circuit comprising:

a first transistor (106) having a control terminal, an input terminal, and an output terminal, wherein said first transistor control terminal is coupled to a first feedback control block output (110) and said first transistor input terminal is coupled to receive a positive supply voltage (Vdd);

a second transistor (102) having a control terminal, an input terminal, and an output terminal, wherein said second transistor control terminal is coupled to receive a data signal and said second transistor input terminal is coupled to said first transistor output terminal;

a third transistor (104) having a control terminal, an input terminal, and an output terminal, wherein said third transistor control terminal is coupled to receive said data signal and said third transistor output terminal is coupled to said second transistor output terminal;

a fourth transistor (108) having a control terminal, an input terminal, and an output terminal, wherein said fourth transistor control terminal is coupled to a second feedback control block output (112), said fourth transistor output terminal is coupled to said third transistor input terminal, and said fourth transistor input terminal is coupled to receive a supply voltage less positive than said positive supply voltage (Vss).

the first feedback control block (110) having an input and said first feedback control block output, wherein said first feedback control block input is coupled to said second transistor output terminal; and

the second feedback control block (112) having an input and said second feedback control block output, wherein said second feedback control block input is coupled to said third transistor output terminal. The feedback control blocks are resistors.

Regarding claims 17, figure 1 of Michail shows a method comprising:

receiving an input signal (Input);

driving at least one transistor in a stacked output transistor array having two or more transistors (102, 104, 106, 108);

sampling an output of the stacked output transistor array (feedback blocks 110, 112); and

transferring a signal based on said sample of the stacked output transistor array to one or more transistors (106, 108) in said stacked output transistor array.

Regarding claims 18, 19, 20 and 21, figure 1 of Michail shows a method comprising:

generating an output signal;

receiving said output signal; and

feedback a signal based on said received output signal to at least one transistor (106, 108) in a stacked output transistor array having two or more transistors (102, 104, 106, 108). The feedback devices (110, 112) comprise resistors. In figure 1 of Michail, the output signal is "compared" with the reference voltage (Vss) by the resistive networks and "said stacked output transistor array substantially generated said output signal".

Regarding claims 22 and 23, figure 1 of Michail shows a method comprising:

receiving an input signal;

driving at least one transistor (PMOS 102) in a first stacked output transistor array (102, 106) having two or more transistors at a first time (the low period of the input signal);

driving at least one transistor (NMOS 104) in a second stacked output transistor array (104, 108) having two or more transistors at a second time (the high period of the input signal);

sampling an output of said first stacked output transistor array and said second stacked transistor array; and

transferring a signal based on said sample of said first stacked output transistor array and said second stacked output transistor array to one or more transistors (106, 108) in said first stacked output transistor array.

Regarding claims 24-27, figure 1 of Michail shows a method comprising:

driving one or more transistors (102, 104) connected in series to produce an output;

feeding back to said one or more transistors a portion of said output (resistive dividers 110, 112). The feedback devices are resistors. Transistors (102) and (104) are connected to the output. Transistor (106) is connected directly to supply voltage (Vdd).

Regarding claims 28-30, figure 1 of Michail shows an apparatus comprising:

a first transistor (106) having a source, a drain, and a gate wherein said first transistor source is connected to a voltage (Vdd);

a second transistor (102) having a source, a drain, and a gate wherein said second transistor source is connected to said first transistor drain, said second transistor gate is connected to an input, and said second transistor drain is an output;

a feedback device (110) having an input and an output, said feedback device input connected to said output, and said first transistor gate connected to said feedback device output. The feedback device is selected from the group consisting of a resistor.

Regarding claims 8 and 16, the recitation "a machine-readable medium" is merely an intended use. It has been held that a recitation with respect to the manner in which a

claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQF.2d 1647 (1987). The driver circuit of the present application can be used in any electronic system. Therefore, the limitation "a machine-readable medium" has not been given patentable weight.

Allowable Subject Matter

Claims 10-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 10-14 are objected to because the prior art of records (USP. 5,760,649) fails to teach or suggest a circuit comprising a fifth and a sixth transistor as called for in claims 10 and 12; a feedback control block comprising a transmission gate as called for in claims 13 and 14.

Response to Arguments

In the Remarks, page 11, the Applicant argues that "he feedback network 110, 112 provide a bias irrespective to the output because the feedback is tied to Vss and Vdd". In fact figure 1 of Michail shows that the feedback circuits (blocks) 110 and 112 are the **voltage dividers** that feedback part of the output voltage to the output driver stage (102, 104 106, 108). **The feedback signals control the gain and linearity of the output driver** (col. 3, lines 41-46; col. 4 lines 21-23). The feedback blocks (110) and (112) senses the output voltage of the driver and the **voltage divider blocks** comprises resistors (114, 116, 118 and 120). The values of the feedback signal depends on the value of the output signal with respect to the supply voltage Vdd and the ground Vss. For clarification, the feedback signals can be expressed as followed: the feedback signal applied to gate of transistor (106) is [Vout/114+116)]*116 and the feedback voltage applied to the gate of transistor (108) is [[(Vout-Vdd)/118+120]*118] +Vout.

On page 12, the Applicant argues that "Michail discloses the feedback network being connected to supply voltage. These are not anticipated Applicants' s claim 9". Claim 9 merely recites "first feedback control block " and "second feedback control block ". Michail shows first

feedback control block (110) and second feedback control block (112). The Applicant does not recite the special structures of the first and second feedback control blocks that are distinguished from the first and second feedback control blocks of Michail. The same rationale is applied to claims 17, 18, 24 and 28.

Regarding to claims 20 and 24 the Applicant fails to explain how the "received output signal" is compared to " a reference voltage". In claim 24, the recitation " a portion of said output" is misdescriptive because there is no dividing device shown in figure 7 that fed **a portion of the output signal** to the transistor(s). Thus, the rejection under 112, 2nd remains.

Conclusion

Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen

12-13-05

TUAN T. LA...
PRIMARY EXAMINER